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Journal of Crystal Growth 279 (2005) 229–240
JOURNAL OF CRYSTAL GROWTH
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Importance of pulse reversal effect of CdSe thin films for optoelectronic devices

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Received 17 December 2004; accepted 11 February 2005
Available online 26 April 2005
Communicated by K.W. Benz

Abstract

Systematic studies of cadmium selenide thin films were prepared by without and with pulse reversal plating technique. In the present work, preparation of CdSe thin films was reported with lower duty cycle and pulse reversal effect. Due to these effects electrical and opto-electronic property of the material were changed. The thin film of CdSe was deposited on cleaned conducting substrates like titanium, SnO_2, nickel and stainless steel, respectively. The pulse plated CdSe films without and with pulse reversal films were heat treated and characterized by XRD, optical studies, scanning electron microscopy and photo electrochemical properties. Semiconductor parameters were estimated for without and with pulse plating technique. The barrier height Φ_b was calculated for CdSe deposited on different conducting substrates.

Keywords: A3. Pulse plating; A3. Pulse reversal; A3. Thin film; B1. CdSe; B2. Semiconducting material; B3. Opto electronic devices

1. Introduction

Amongst the II–VI semiconductors, CdSe and CdTe have special applications in various solid-state devices in view of their band gaps 1.70 and 1.45 eV, respectively. Based on the results of CdSe-MIS type solar cells yield respectable efficiencies. Conversion efficiency of 16.7% has been released from the single crystal photo anodes. Solar cells from CdSe single crystal are supposed to be very expensive; hence it is desirable to use the large area semiconductor thin film.

Techniques such as vacuum evaporation, spray pyrolysis, electrodeposition have been attempted successfully for the preparation of thin CdSe films. Although the pulse electrodeposition technique in the preparation of CdSe employed higher duty

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doi:10.1016/j.jcrysgro.2005.02.020

cycles earlier, the present preparation employs it for the lower duty cycle and a systematic study of without and with pulse reversal effect. Results on the structural, optical, electrical, PEC properties and Schottky barrier effect of these films are reported and discussed.

The characteristics of the films deposited by pulse electrodeposition are controlled by factors like on-time, off time and current density [1–3]. Pulse plating technique has distinct advantages compared to conventional electrodeposition namely, crack free, hard deposits and fine grained films with more uniformity, lower porosity and better adhesion. CdSe films were also deposited by inverting the pulse voltage/pulse current from cathodic to anodic during a small fraction of the total period (pulse reversal). The main purpose of pulse reversal is to remove species preferentially from areas that tend to over plate during the cathodic part of the cycle [4]. Changes in deposit structure; mainly affects the grain size, because of forced nucleation at each new cathodic pulse. It is clear that adsorption, desorption as well as re-crystallization take place with every new pulses. The main purpose of carrying out pulse reversal plating [5] is to obtain better film thickness with good adherence which in turn will yield higher grain size due to better nucleation sites. As a result, high conversion efficiencies [6] for photo-electrochemical cells fabricated with the usage of these films.

2. Experimental procedure

CdSe films of area 2.5 cm^2 were deposited on titanium, indium tin oxide (ITO), stainless steel, and nickel substrates at different duty cycles in the range 6.25–50%. AR grade cadmium sulfate and selenium dioxide were the precursors for the deposition bath, pH was adjusted to a value of 2 by the addition of dil. H_2SO_4. The pulse voltage/pulse current, concentration and pH were optimized using the earlier reports [7]. Under optimized condition, a concentration of 0.5 M of $CdSO_4$, 0.1 M of SeO_2 was taken. The deposition was carried out for duration of one hour, at −900 mV (SCE) [8,9] at room temperature. The thickness of the films was estimated to be 1.6 μm for as deposited by gravimetric method. The films were heat treated in air at different temperatures in the range of 450–550 °C for duration of 5 min. The thickness of the films after heat treatment was around 1.5 μm. Depositing about six sets of samples under each condition checked reproducibility of the deposition process.

Structural analysis was made on the CdSe films deposited at different duty cycles (both as deposited as well as post-heat treated). All the surfaces of the films were smooth and adhere firmly to the substrate. Identification of the materials was made by X-ray diffraction using CuK_α radiation ($\lambda = 1.541$ Å) JEOL 8030 model X-ray diffractometer. By using the same X-ray pattern, the full widths at half maximum (FWHM) for all the films were obtained. Phase identification was made and crystallite size of the films was determined from Scherer's equation [10].

Surface morphology of the films deposited on titanium substrates was studied by using JEOL JSM 35CF model SEM. The equipment had a maximum magnification of 1,80,000 with a resolution of 60 Å.

Optical absorption studies were carried out on the films deposited on ITO at different duty cycles and heat treated at 550 °C in air for 5 min (containing single phase hexagonal CdSe). The absorption coefficient [11] was calculated from the absorption spectroscopy by using Hitachi UV-VIS-NIR spectrophotometer.

Photo electrochemical (PEC) cells were prepared using the films deposited on titanium substrates with different duty cycles heat-treated at 550 °C in air. The films were lacquered with polystyrene in order to stop off the metal substrate portions from being exposed to the redox electrolyte. These films were used as the working electrode. Graphite was used as the counter electrode. The electrolyte was 1 M polysulfide (1 M NaOH, 1 M Na_2S, 1 M S). This electrolyte was chosen as it is well known that CdSe electrode has reasonable stability and can yield respectable photo outputs in polysulfide, the light source used for illumination was an ORIEL 250 W tungsten halogen lamp.

Changing the distance between the source and the cell varied the intensity of illumination. The power output characteristics of the cells were measured by connecting a resistance box and an ammeter in series; the voltage output was measured across the load resistance. The photocurrent as well as dark current was measured with a HIL digital multimeter. A HIL digital multimeter measured the output voltage. The photocurrent and photo voltage was calculated as the difference between the current and potential values under dark and under illumination respectively.

Photo etching was carried out by shorting the photo electrodes and the graphite counter electrode under an illumination of $100\,\mathrm{mW\,cm^{-2}}$ in 1:100 HCl for different duration ranges from 0 to 40 s.

Semiconductor parameter like flat band potential V_{fb}, carrier concentration N_d, Band bending V_b, depletion layer width W, doping density of states in conduction band N_c, conduction band E_c, Fermi level E_f of the semiconductor, values band E_v, band gap E_g was estimated.

Spectral response measurements were carried out on the photo electrodes prepared with and without pulse reversal by using a photo physics monochromator and a 250 W tungsten halogen lamp, 1 M polysulfide as electrolyte, graphite as counter electrode and the photo electrode as the working electrode. The wavelength was varied in the range 550–850 nm and the photocurrent was noted at each wavelength.

These photocurrent values were used for calculation of the quantum efficiency (ϕ) using the well-known relation [12],

$$\phi = \frac{1240 J_{sc}}{\lambda P_{in}}, \tag{1}$$

where J_{sc} is the photocurrent, λ is the wavelength of illumination, P_{in} is the power of light incident on the photo electrode.

The conduction mechanism in semiconductors can be understood by analyzing current–voltage (I–V) plots. For single carrier injection at low voltages, the plot is generally a straight line showing the validity of Ohm's law. However, at higher voltages some deviation is expected. The voltage was applied using a DC power supply APLAB. The applied voltage varied in the range from 0 to 2.5 V.

3. Results and discussion

3.1. XRD studies

X-ray diffractograms of the films deposited at different duty cycles are shown in Fig. 1. The X-ray diffractograms indicate the polycrystalline nature of the films. In all the figures the prominent peaks corresponding to (1 1 1), (2 2 0) and (3 1 1) reflections of CdSe was observed at 2θ of 25.2°, 42.0° and 49.6° respectively. Two peaks corresponding to Ti (2θ of 53.2° and 70.5°) and one peak corresponding to Cd were also observed. The as deposited films exhibit cubic structure with preferential orientation in the (1 1 1) direction. As the duty cycle decreases, the intensity of the peaks are also observed to decrease, the width of the (1 1 1) peak is also observed to increase with decrease of duty cycle for an increase of OFF time from 1 to 15 s. As the OFF time increases the number of peaks are observed to decrease gradually and for OFF times greater than 15 s only peaks corresponding to Cd were observed along with the Ti peaks. Hence, films were prepared only with OFF times $\leqslant$15 s. The thickness of the films were also found to be increased as the OFF time decreases, that could be understood, since the number of pulses increased for the same total duration of deposition viz., 1 h.

In order to change the phase from cubic to hexagonal (which is the desired phase for optoelectronics applications), the films were heat treated in air at different temperatures in the range 450–550 °C [9] for 10 min. As the temperature increased from 450 °C peaks corresponding to hexagonal CdSe are shown in Figs. 2 and 3. At a heat treatment temperature of 550 °C only single phase hexagonal CdSe reflection corresponding to (1 0 0) (0 0 2) (1 0 1) (1 0 2) (1 1 0) (1 0 3) (1 1 2) (2 0 3) (1 0 5) and (3 0 0) at $2\theta = 23.9$, 25.4, 27.0, 35.2, 42.0, 45.8, 49.4, 63.7, 70.8, and 76.3 were observed along with four titanium peaks.

The films deposited with different pulse reversal times in the range 30–90 ms indicated hexagonal

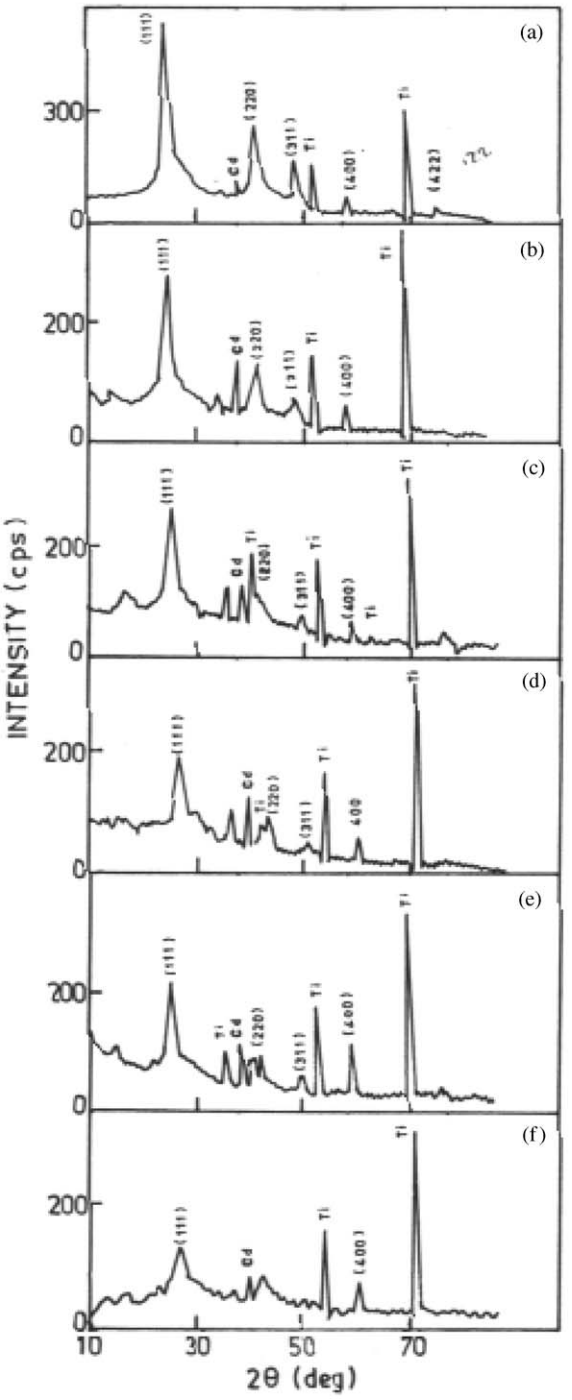

Fig. 1. XRD pattern of pulse plated CdSe films on titanium substrate for different duty cycle (a) conventional, (b) 50%, (c) 33%, (d) 15%, (e) 9% and (f) 6.25%.

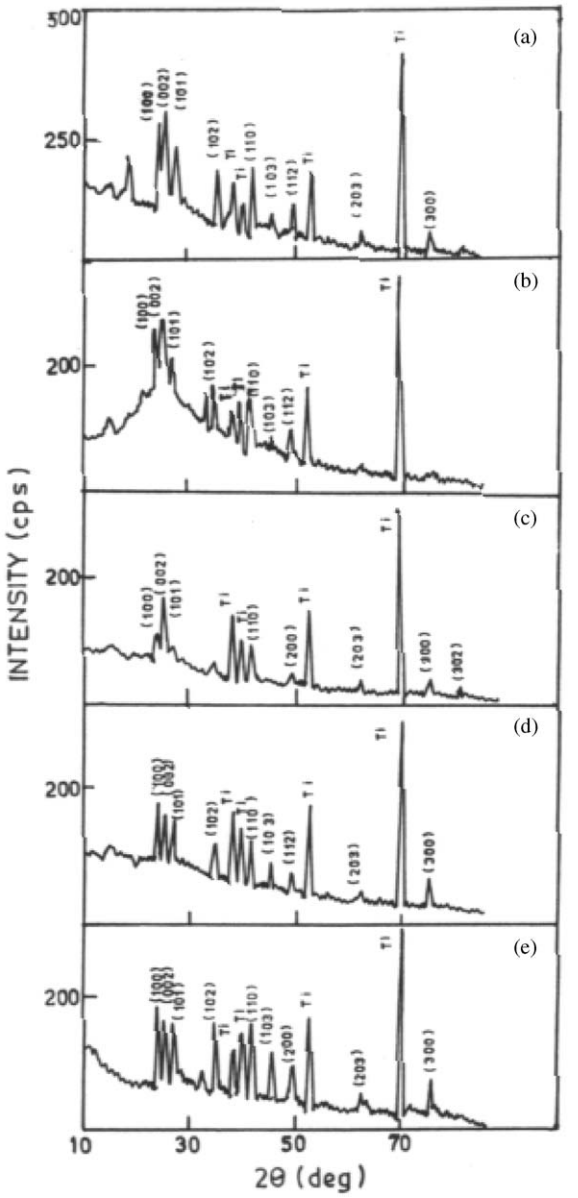

Fig. 2. XRD pattern of pulse plated CdSe films on titanium substrate for different duty cycle and annealed at 525 °C (a) 50%, (b) 33%, (c) 15%, (d) 9% and (e) 6.25%.

phase in their X-ray diffraction patterns (Fig. 4). The intensity of the peak (1 0 0) reflection was found to be increased with reversal time varied from 30 to 90 ms.

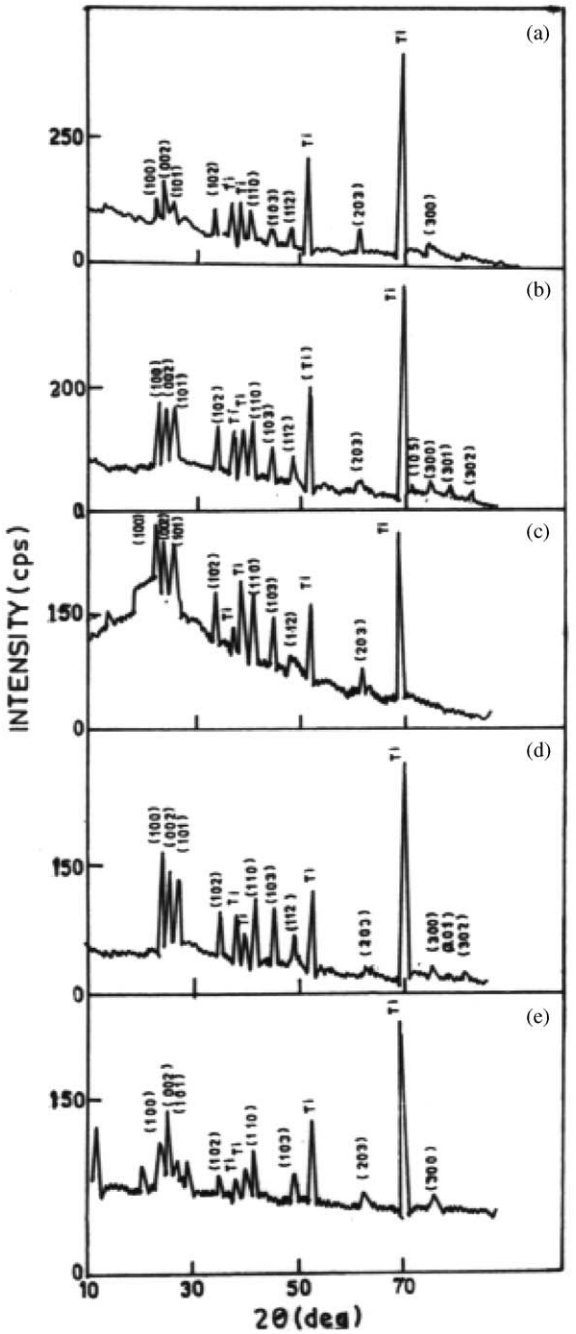

Fig. 3. XRD pattern of pulse plated CdSe films on titanium substrate for different duty cycle and annealed at 550 °C (a) 50%, (b) 33%, (c) 15%, (d) 9% and (e) 6.25%.

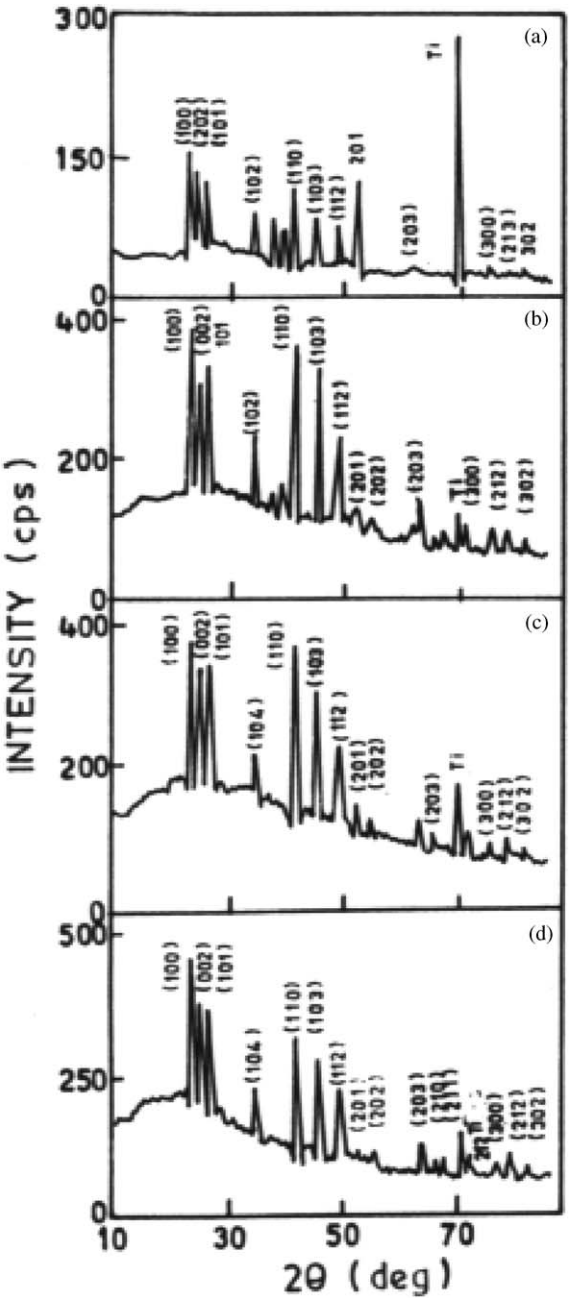

Fig. 4. XRD pattern of the CdSe films for different pulse reversal timings (a) 1:10, (b) 1:10:30 ms, (c) 1:10:60 ms and (d) 1:10:90 ms.

3.2. SEM studies

Fig. 5a shows the scanning electron micrograph (SEM) of the uncoated titanium substrate. From the micrograph, uniform distributions of fine grains are observed. Fig. 5b–f shows the micrographs of the CdSe films deposited using different duty cycles. It was observed that as the duty cycle decreases, the grain size decreases; very fine grains were seen for the films deposited at a duty cycle of 6.25%. This was also supported by the X-ray diffraction results, wherein the FWHM was wide for the films deposited at a duty cycle of 6.25%. After heat treatment at 550 °C, irrespective of the duty cycle, the grain size was found to be increased compared to the as deposited films. Large grains ($>5\,\mu m$) were observed for the post heat-treated films deposited at duty cycles greater than 10%. For the films deposited at 50% duty cycle, cube shaped crystallites were observed Fig. 5g–k. The films deposited at 9% with pulse reversal exhibit large flaky crystallites with improved crystallinity (Fig. 5l). After photo etching the film, the grain boundaries were clearly visible (Fig. 5m).

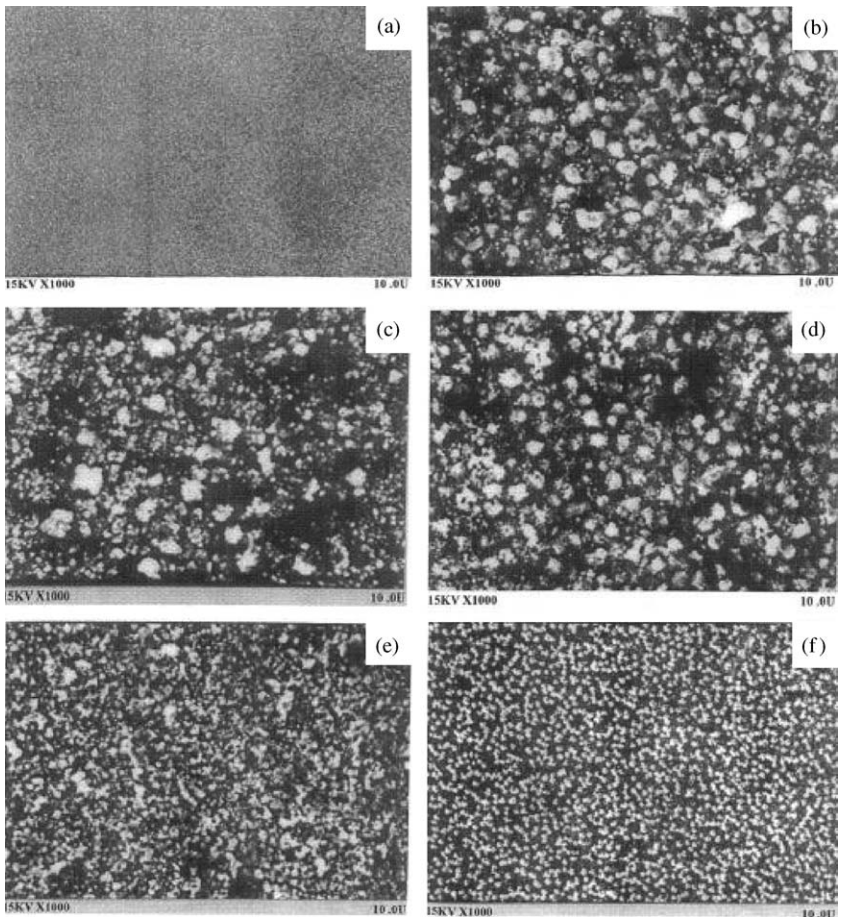

Fig. 5. (a–f). SEM photographs of pure titanium substrate and as prepared CdSe deposited on titanium for different duty. (a) Titanium, (b) 50%, (c) 33%, (d) 15%, (e) 9% and (f) 6.25%. (g–k). SEM photographs CdSe deposited on titanium substrate for different duty cycle and annealed at 550 °C (g) 50%, (h) 33%, (i) 15%, (j) 9% and (k) 6.25%. (l–m). SEM photographs of pulse reversal CdSe films at 9% duty cycle and annealed at 550 °C.

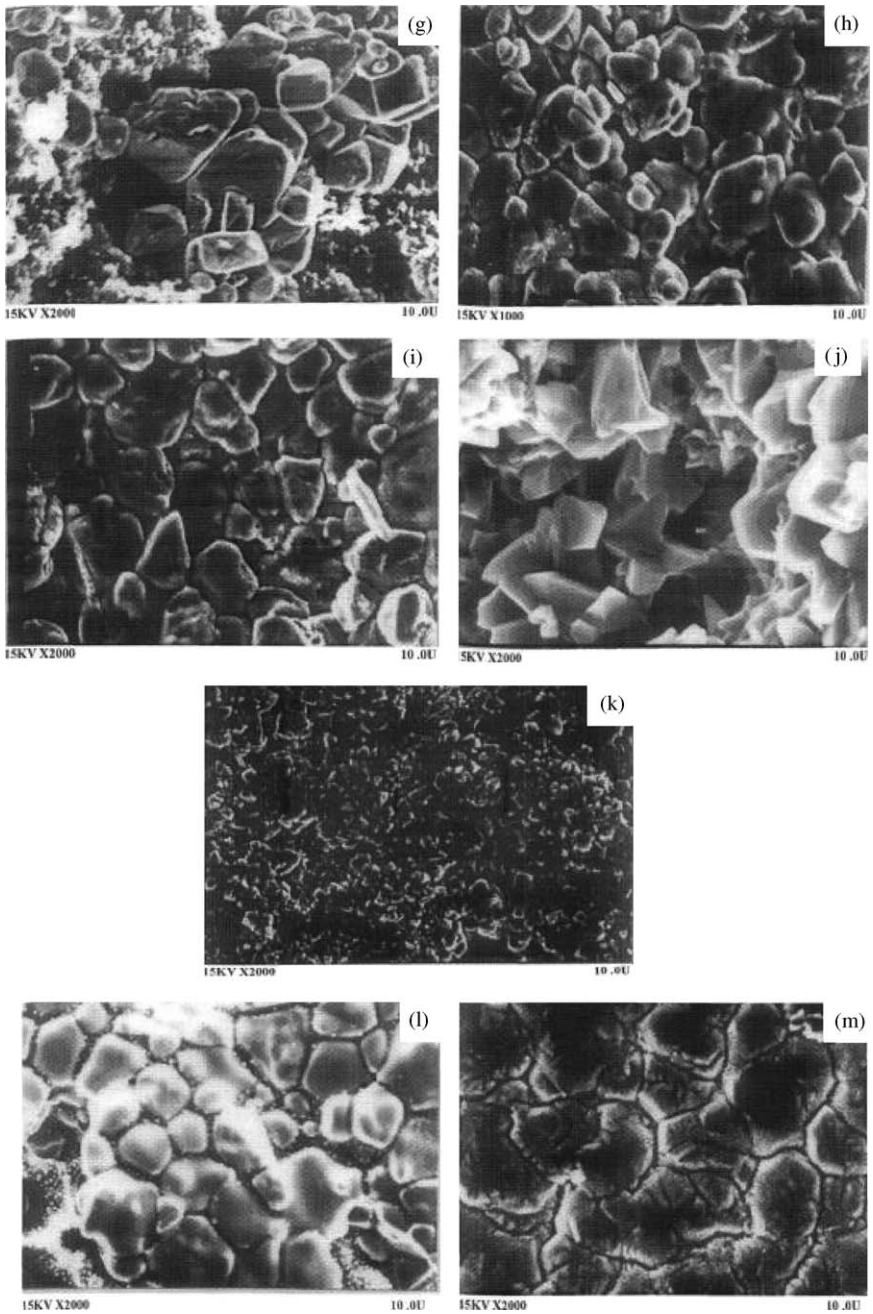

Fig. 5. (*Continued*)

3.3. Optical absorption measurements

The band gap of the films was determined by plotting a graph between $(\alpha h\nu)^2$ and $h\nu$. The extrapolation of the linear region to the $h\nu$ axis showed the band gap of the material. Fig. 6 indicates the direct band gap of 1.70 eV for the films annealed at 550 °C irrespective of the duty

cycle. An absorption coefficient of $10^4\,cm^{-1}$ was obtained [13].

3.4. Pulse without and with etching

The power output characteristics of the PEC cells were made using the photo electrodes deposited at different duty cycles and post heat treated at 550 °C. As the duty cycle increases, both V_{oc} and J_{sc} were found to be increased up to a duty cycle of 9%, beyond which the photocurrent decreases, this is due to the high resistance of the films deposited at these duty cycles [4,6,9] (Table 1).

Photo etching was carried out by shorting the photo electrodes and the graphite counter electrode under an illumination of $100\,mW\,cm^{-2}$ in 1:100 HCl for different durations in the range 0–40 s. Both photocurrent and photo voltage were found to be increased up to 30 s photo etch, beyond which they begin to decrease. This is illustrated in Fig. 7(a, b). The decrease of the photocurrent and photo voltage is attributable to separation of grain boundaries due to prolonged photo etching [14].

In both photo etched and unetched electrodes, the films deposited with a duty cycle of 9% exhibit maximum photo activity. Samples deposited with higher duty cycles exhibited lower PEC output, since the thicknesses of the films were less and moreover the films contained mixed phases of Cd and CdSe as evident from X-ray diffractograms.

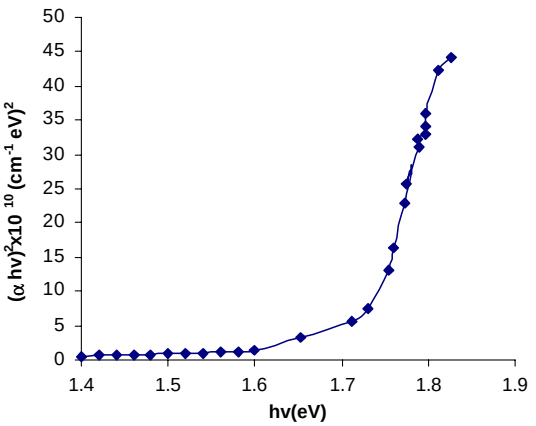

Fig. 6. $(\alpha hv)^2$ vs. hv plot for pulse plated CdSe heat treated at 550 °C.

3.5. Pulse reversal without and with etching

The power output characteristics of the PEC cells made using the pulse plated films with and without pulse reversal and etched were determined. Both V_{oc} and J_{sc} were found to be increased up to 60-ms pulse reversal, beyond which they decrease due to decrease in thickness of the film. The electrodes were photo etched for different duration in the range 5–40 s, the V_{oc} and J_{sc} values were found to be increased up to 30 s photo etch as shown in Fig. 8(a, b) beyond which there was a reduction in these values. Hence, a photo etching time of 30 s was maintained. The load characteristics of the above samples were studied at $80\,mW\,cm^{-2}$ illuminations. Fig. 9 shows the power output characteristics of the electrodes prepared with and without pulse reversal after photo etching. The J_{sc} is found to be increased from $13.56\,mA\,cm^{-2}$ for films deposited without pulse reversal i.e. for 1:10% to $2.35\,mA\,cm^{-2}$ [9]

Table 1
PEC characteristics of pulse plated CdSe films heat-treated at 550 °C

Duty cycle (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	*ff*	η (%)	R_s (Ω)	R_{sh} (kΩ)	*n*
Before photo etching							
1:10	350	4.57	0.38	0.88	51	1.59	1.08
1:10:60	360	7.08	0.39	1.46	48	1.50	1.53
After photo etching							
1:10	377	13.56	0.44	3.20	42	1.31	1.96
1:10:60	396	22.35	0.40	6.57	36	1.26	2.08

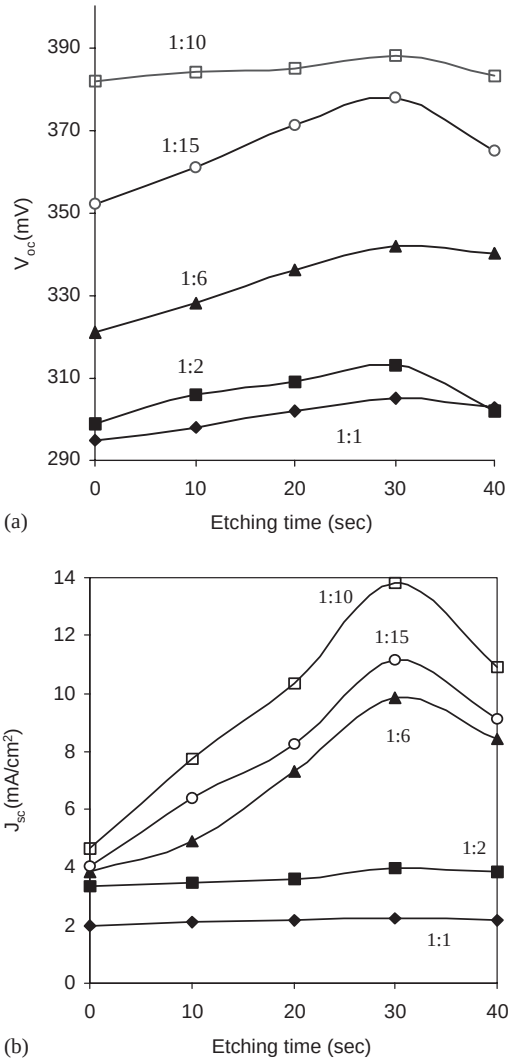

Fig. 7. Without pulse reversal of CdSe films deposited at 9% duty cycle. (a) Photo etching time vs. V_{oc} for different dusty cycles (♦)—1;1, (■)—1:2, (▲)—1:6, (□)—1:10, (○)—1:15, (b) Photo etching time vs. J_{sc} for different dusty cycles (♦)—[1:1]50%, (■)—[1:2]33%, (▲)—[1:6]15%, (□)—[1:10]9% and (○)—[1:15]6.25%.

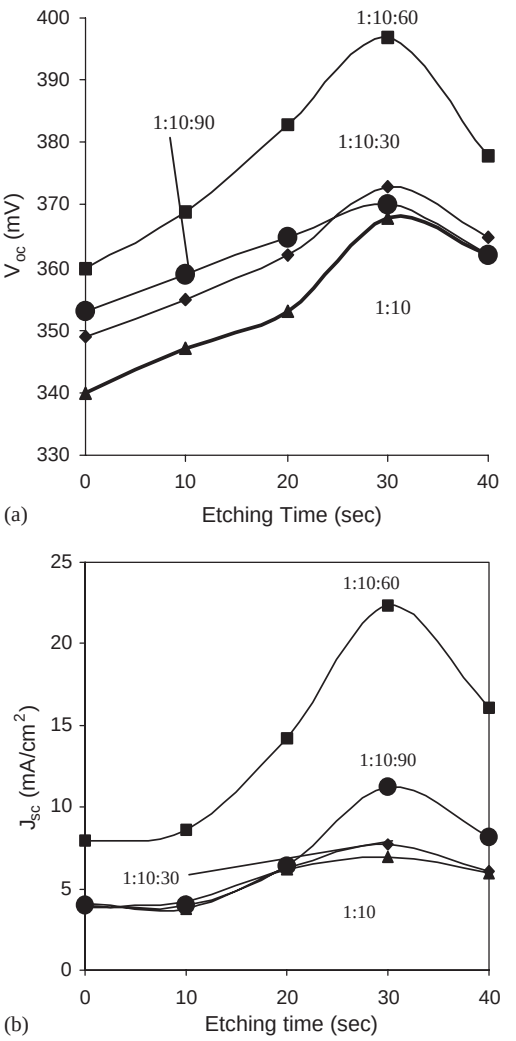

Fig. 8. With pulse reversal of CdSe films deposited at 9% duty cycle (a) Photo etching time vs. V_{oc} for different duty cycle (▲)—1:10, (♦)—1:10:30 ms, (■)—1:10:60 ms, (●)—1:10:90 ms, (b) Photo etching time vs. J_{sc} for different duty cycles (▲)—1:10, (♦)—1: 10:30 ms, (■)—1:10:60 ms and (●)—1:10:90 ms.

for the films deposited with pulse reversal of 1:10:60 ms. It appears that the improved characteristics were due to the improvement in crystallinity and grain size as evident from the X-ray diffraction and SEM data. The variation of J_{sc} and V_{oc} with intensity was also studied, both the parameters were found to be increased with intensity. A plot of ln J_{sc} vs. V_{oc} (Fig. 10) yielded a value of 1.31 for the ideality factor and 3.5×10^{-6} cm for the reverse saturation current.

3.6. Quantum efficiency

Plots of ϕ vs. λ are shown in Fig. 11. The plots indicate maximum at 720 nm corresponding to the

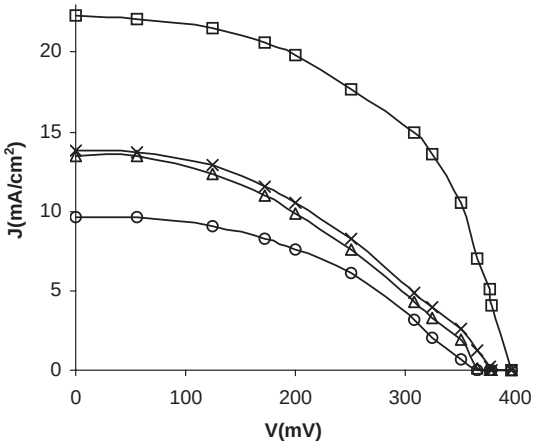

Fig. 9. Power output characteristics of the CdSe thin film electrodes prepared with and without pulse reversal after photo etching. (a) 1:10, (b) 1:10:30 ms, (c) 1:10:60 ms and (d) 1:10:90 ms.

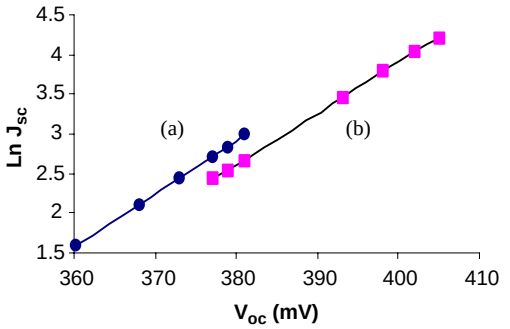

Fig. 10. $\ln J_{sc}$ vs. V_{oc} plot for without and with pulse reversal (a) 1:10 and (b) 1:10:60 ms.

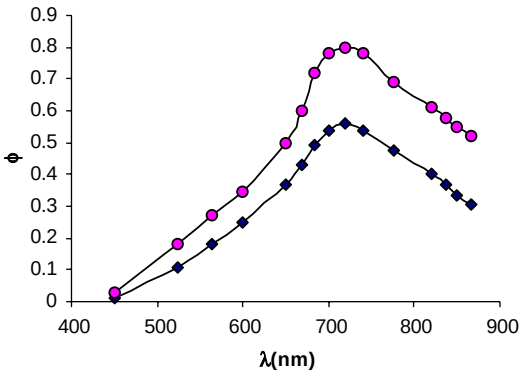

Fig. 11. Plot of ϕ vs. λ without and with pulse reversal CdSe films.

band gap of the material, this matches well with the band gap obtained from optical absorption measurements. While a quantum efficiency of 0.56 was obtained for films deposited without pulse reversal, the quantum efficiency 'ϕ' 0.80 was obtained for the electrodes prepared with pulse reversal.

The values of α and ϕ were used to plot α^{-1} vs. ϕ^{-1} and the value of minority carrier diffusion length L_n [16] was estimated from the slope of the plot. The estimated values of ϕ and L_n were compared with the earlier reports and listed in Table 2.

The main shortcoming of polycrystalline photo electrodes is recombination at grain boundaries, which is an important source of efficiency losses. This is certainly the case for as-electrodeposited CdSe films, where the grain size (d) is about two orders of magnitude lower than the light penetration depth ($1/\alpha$). Therefore, the first beneficial effect of annealing is to increase the crystallite size, so that $d > 1/\alpha$.

As in the case of CdS, electronic conduction mechanisms in CdSe are associated to lattice Se vacancies (V_{Se}) that are known to behave both as shallow donor centers and deep electron traps [18].

Selenium vacancies are generated as a result of partial electrode evaporation during annealing. Annealing temperature was high, greater V_{Se} and N_d, and so the width 'W' was thinner. At higher temperatures ($>550\,^{\circ}C$), though N_d increases, L_P is observed to decrease, since increasing concentration of V_{Se} results in V_{Se} behaving as recombination centers [18].

For an efficient control of V_{Se} and N_d, the annealing treatment has to be performed in an inert atmosphere (eg. He) contains a few ppm of

Table 2
Variation of L_n & ϕ with respect to duty cycle

Duty cycle (%)	λ_{max} (nm)	L_n (μm)	ϕ
1: 10	720	0.45	0.56
1:10:30	722	0.86	0.61
1:10:60	720	0.25	0.80
1:10:90	719	0.77	0.75

oxygen in order to facilitate oxygen chemisorptions. Chemisorbed oxygen behaves as an efficient electron acceptor [18] able to compensate the excess concentration of free electrons, which result in an efficient control of N_d. This effect is pronounced when, after annealing, the electrode is heated in H_2 atmosphere at 200 °C; the oxygen gets desorbed electrons are freed and N_d should increase. For low annealing temperatures, the recombination dominating mechanism occurs at grain frontiers with participation of impurities (especially chemisorbed O_2) [18]. However, at high enough temperatures (>550 °C), recombination at the grain interface region becomes negligible and L_p is more affected by chemisorbed O_2. The effect of photo etching is to remove the CdO layer formed at the surface during annealing, but even after photo etching, the CdSe grains rich in oxygen remain in tact with the electrolyte. Due to the fact that the strength of Cd–Se bond is higher than the Cd–O bond, the localized energy levels associated to Cd^{2+} ions linked to oxygen in the CdSe lattice are below the conduction band, behaving as deep traps for electrons.

3.7. Semiconductor parameters and barrier height measurements

I–V characteristics of the films deposited on different substrates like stainless steel, nickel and titanium are shown in Fig. 12a–c. Semiconductor parameter like flat band potential V_{fb}, carrier concentration N_d, Band bending V_b, depletion layer width W, doping density of states in conduction band N_c, conduction band E_c, Fermi level E_f of the semiconductor, values band E_v, band gap E_g have been estimated and the results are shown in Table 3.

The barrier height for the films deposited on different substrates is indicated in Table 4. The barrier heights have been calculated. From the table it is clear that titanium possessing a work function very close to CdSe, behaves as an ohmic contact to CdSe, whereas the other two contacts nickel and stainless steel have work functions are not ohmic to CdSe, due to the difference in work function.

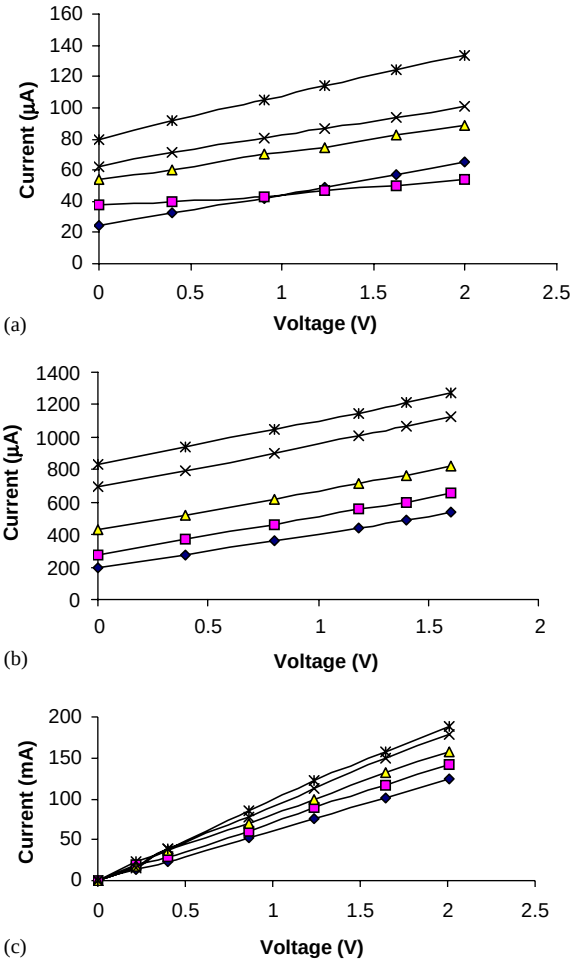

Fig. 12. I–V characteristics of pulse plated CdSe films for different duty cycles on (a) Ti, (b) stainless steel and (c) nickel.

4. Conclusion

This work has investigated the influence of pulse plated CdSe films without and with pulse reversal effect that changes the morphology of the films. The enhancement of the photo electrochemical properties have been achieved due to the effect of pulse reversal with an optimized reversal time of 60 ms. Semiconductor parameters and the barrier height measurement have been tested for different conducting substrates. Titanium shows ohmic behavior and the other two substrates nickel and stainless steel act as rectifying contact for CdSe

Table 3
Semiconductor parameter for CdSe deposited on different substrate and heat-treated at 550 °C

Semiconductor parameters	Titanium	Stainless steel	Nickel
1. Flat band potential (V_{fb}) V_{SCE}	1.200	1.168	1.14
2. Carrier concentration $\times 10^{15}\,cm^{-3}$ (N_d)	7.045	0.047	0.081
3. Band bending (V_b) V_{SCE}	−0.61	−0.578	−0.55
4. Depletion layer width (W) μm	0.9	0.11	0.086
5. Doping density of states in conduction band (N_c) $\times 10^{24}\,m^{-3}$	1.1723	1.1723	1.1723
6. Conduction band edge (E_c) eV	1.1546	1.161	1.1315
7. Fermi level E_f of the semiconductor	−0.0454	−0.05197	−0.0431
8. Valency band edge (E_v) eV	0.5454	0.539	0.604
9. Band gap (E_g) eV	1.70	1.70	1.70

Table 4
Values of barrier height for CdSe films deposited at different duty cycle on nickel, stainless steel and titanium

Duty cycle	Barrier height ϕ_b (eV)		
	Nickel	Stainless steel	Titanium
50.0	0.49	0.40	Ohmic
33.3	0.49	0.40	Ohmic
15.1	0.48	0.39	Ohmic
9.9	0.48	0.39	Ohmic
6.2	0.48	0.39	Ohmic

films. Preparations of the nano materials can be achievable by choosing the suitable duty cycle, ON time and OFF time with period of micro/nano seconds.

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